



#### United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER OF PATENTS AND TRADEMARKS Washington, D.C. 20231 www.ispio.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/832,272	04/10/2001	Kirk Prall	3969.3US (95-0310.3)	2827	
24247	7590 02/26/2003				
TRASK BRITT			EXAMINER ·		
P.O. BOX 2550			WARREN, MATTHEW E		
SALT LAK	E CITY, UT 84110	WARREN, MET THEW B			
			ART UNIT	PAPER NUMBER	
		·	2815		
			DATE MAILED: 02/26/2003		

Please find below and/or attached an Office communication concerning this application or proceeding.

·		Application No.	Applicant(s)				
Office Action Summary		09/832,272	PRALL ET AL.	W			
		Examiner	Art Unit				
		Matthew E. Warren	2815				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply							
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).  - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).  Status							
1) 🖾	Responsive to communication(s) filed on 27 /	November 2002 .					
2a)⊠	-	is action is non-final.					
3)							
Disposition of Claims							
4)⊠	Claim(s) $\underline{1-42}$ is/are pending in the application						
	4a) Of the above claim(s) is/are withdrawn from consideration.						
5)	Claim(s) is/are allowed.						
6)⊠	6)⊠ Claim(s) <u>1-42</u> is/are rejected.						
7)	Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/or election requirement.  Application Papers							
9)☐ The specification is objected to by the Examiner.							
10) ☐ The drawing(s) filed on is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.							
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
11)☐ The proposed drawing correction filed on is: a)☐ approved b)☐ disapproved by the Examiner.							
If approved, corrected drawings are required in reply to this Office action.							
12)☐ The oath or declaration is objected to by the Examiner.							
Priority under 35 U.S.C. §§ 119 and 120							
13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).							
a) ☐ All b) ☐ Some * c) ☐ None of:							
	1. Certified copies of the priority documents have been received.						
	2. Certified copies of the priority documents have been received in Application No						
<ul> <li>3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).</li> <li>* See the attached detailed Office action for a list of the certified copies not received.</li> </ul>							
* See the attached detailed Office action for a list of the certified copies not received.  14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).							
a) The translation of the foreign language provisional application has been received.							
15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.							
Attachmer		🗖	(DTO 442) P 1	0(5)			
2) Notice	ce of References Cited (PTO-892) ce of Draftsperson's Patent Drawing Review (PTO-948) mation Disclosure Statement(s) (PTO-1449) Paper No(s) _	5) Notice of Inform	nary (PTO-413) Paper No nal Patent Application (P				

Application/Control Number: 09/832,272

Art Unit: 2815

### **DETAILED ACTION**

This Office Action is in response to the RCE and Response filed on November 27, 2002.

# Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al. (US 5,629,539) in view of Iacoponi (US 5,545,592).

Aoki et al. shows (fig. 1b) a dynamic random access memory array (DRAM) comprising a substrate (10), a plurality of memory cells, each cell having field effect access transistors and a stacked capacitor (21b, 27, and 28). The field effect transistors have source/drain regions (15b) that function as storage node junctions and are connected to the capacitor of the memory cell. The transistors also have second source/drain regions (15a) which functions as an access node junction and an insulated gate (13) overlying the substrate. The gate is insulated from the substrate by a gate dielectric (12) of silicon oxide and has vertical sidewalls (16) and an upper surface which are both covered by a dielectric of nitride (14). The gate electrode (13) comprises doped polysilicon. Along the length of the substrate, other access transistors are insulated from the substrate by a field oxide region (11). An interlevel dielectric layer

(31) comprising a second dielectric material is blanketed over the substrate to a level above the capacitors. A plurality of digit line contact openings (having 21a and 24a) penetrate the interlevel dielectric layer and terminate at an access node junction (15a). The contact opening is self-aligned with the first dielectric material of the sidewall insulation of the gate because the contact is adjacent to the gate. The contact opening may be filled with a layered structure including tungsten and titanium (col. 8, lines 40-46) A digit line (33) is formed on top of the interlevel dielectric layer and makes electrical contact to the tungsten plug. Aoki shows all of the elements of the claims except the digit line contact opening having the specific titanium and CVD TiN and tungsten layer formed on the access node junction. Iacaponi shows (figs. 7) a contact structure comprising a contact opening formed in an interlayer dielectric layer (130). An access node junction (in silicon material 100) has a layer of titanium silicide (120) formed on it. A layer of titanium (150) is formed on the sidewalls of the opening. A CVD titanium nitride layer (160) and CVD tungsten (170) are subsequently deposited to fill the openings (col. 1, line 60 - col. 2, line 4). The silicide layer is formed by reacting the titanium with the source/drain region (col.1, lines 32-34). As can be seen from the figure, the titanium layer is overlying the silicide layer by does not make contact with the tungsten layer. The titanium/titanium nitride combination in conjunction with the silicide layer provides a low resistance electrical contact while the TiN provides a diffusion barrier for the underlying Ti layer and an adhesion promoter for the W layer (col. 1, lines 57 - col. 2, line 4). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the contact opening of Aoki by adding

Application/Control Number: 09/832,272

Art Unit: 2815

a titanium metal layer and silicide to the access node junction of a transistor because lacoponi teaches that such a configuration provides a low resistance electrical connection and adhesion promotion of tungsten.

With respect to the limitations of the CVD (chemical vapor deposited) titanium and tungsten and the reaction of titanium with silicon to form silicide, a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17(footnote 3). See also in re Brown, 173 USPQ 685: In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324: In re Avery, 186 USPQ 116 in re Wertheim, 191 USPQ 90 (209 USPQ 254 does not deal with this issue); and In re Marosi et al, 218 USPQ 289 final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above case law makes clear. "Even though product-by- process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-byprocess claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

Art Unit: 2815

# Response to Arguments

Applicant's arguments filed with respect to claims 1-42 have been fully considered but they are not persuasive. The applicant primarily asserts the references of Aoki et al. and lacoponi cannot be combined due to improper motivation and that the combination is evidence of hindsight reasoning. With respect to the arguments for the improper combination, the examiner believes that references can be combined and that lacoponi shows proper motivation for combining. As stated in the rejection above, lacaponi cures the deficiency of Aoki by disclosing the CVD TiN and tungsten layer formed on the access node junction. Iacoponi teaches that such a configuration provides a low resistance electrical contact while also providing a diffusion barrier as well as an adhesion promoter (col. 1, lines 57 - col. 2, line 4). Both references are analogous to each other because they each deal with contact structures. The processes for making Aoki and lacaponi device may differ from each other, but such differences are irrelevant because the applicant's claims are directed to a semiconductor device. The same device could be made by many different processes, therefore the applicant's arguments concerning the incompatible methods are irrelevant for these claims.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does

Application/Control Number: 09/832,272 Page 6

Art Unit: 2815

not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). Therefore, the cited references show all of the elements of the claims and this action is made final.

#### Conclusion

All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Application/Control Number: 09/832,272

Art Unit: 2815

Page 7

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (703) 305-0760. The examiner can normally be reached on Mon-Thurs, and alternating Fri, 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

MEW

February 11, 2003

EDDIE LEE SUPERVISORY PATENT EXAMINER

TECHNOLOGY CENTER 2800